AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An interconnect architecture comprising:

a first interconnect;

a second interconnect adjacent to the first interconnect;

a first driver to drive a signal on the first interconnect, the first driver powered by a first voltage; and

a second driver to drive a signal on the second interconnect, the second driver powered by a second voltage different than the first voltage.

2. (Original) The interconnect architecture of claim 1, wherein the second voltage is less than the first voltage.

3. (Original) The interconnect architecture of claim 2, wherein the second voltage causes a relative delay between the signals on the first interconnect and the second interconnect.

4. (Original) The interconnect architecture of claim 1, wherein the second voltage reduces a worst-case Miller Coupling Factor (MCF) between each adjacent pair of interconnects and a worst-case delay of each interconnect.

5. (Original) The interconnect architecture of claim 1, wherein the second voltage reduces the average energy dissipation of the interconnect architecture.

6. (Original) An apparatus comprising:

an interconnect structure having a plurality of parallel interconnects; and

a plurality of drivers to drive signals on each of the parallel interconnects, first ones of the drivers powered by a first voltage and second ones of the drivers powered by a second voltage different than the first voltage.

7. (Original) The apparatus of claim 6, wherein the drivers and the interconnects are arranged such that drivers of adjacent interconnects are powered by different voltages.

8. (Original) The apparatus of claim 6, wherein the first ones of the drivers each comprise an inverter circuit having a first transistor coupled to the first voltage and a second transistor coupled to GROUND.

9. (Original) The apparatus of claim 8, wherein the second ones of the drivers each comprise an inverter circuit having a third transistor coupled to the second voltage and a fourth transistor coupled to GROUND.

10. (Currently Amended) A multi-stage interconnect architecture comprising:

a bus invert encoder circuit to receive an input data pattern for each of a plurality of interconnects and to provide encoding of data associated with each of the plurality of interconnects;

~~a delay circuit coupled to the encoder circuit to delay signals based on input data sampling patterns;~~

a first interconnect stage having a first plurality of parallel interconnects; ~~and~~

a second interconnect stage having a second plurality of parallel interconnects; and

a delay circuit coupled to the bus invert encoder circuit and the first interconnect stage to delay signals on a first one of the first plurality of parallel interconnects as compared to signals on a second one of the first plurality of parallel interconnects, the signals being delayed based on switching activities of sampling patterns of signals to be applied to the first and second ones of the first plurality of parallel interconnects.

11. (Original) The multi-stage interconnect architecture of claim 10, wherein the bus invert encoder circuit outputs signals to the delay circuit.

12. (Original) The multi-stage interconnect architecture of claim 11, wherein the delay circuit outputs signals onto the interconnects of the first interconnect stage.

13. (Original) The multi-stage interconnect architecture of claim 10, further comprising time-borrowing flip-flop circuits provided between the first interconnect stage and the second interconnect stage.

14. (Original) The multi-stage interconnect architecture of claim 10, further comprising a bus invert decoder circuit to decode signals having traversed the first interconnect stage and the second interconnect stage.

15. (Original) The multi-stage interconnect architecture of claim 10, wherein the encoder circuit reduces a number of switching activities for each of the interconnects.

16. (Original) An electronic system comprising:

a memory component to store data; and

a chipset coupled to the memory component to receive the data and perform an operation on the data, wherein the chipset comprises:

a first interconnect;

a second interconnect adjacent to the first interconnect;

a first driver to drive a signal on the first interconnect, the first driver powered by a first voltage; and

a second driver to drive a signal on the second interconnect, the second driver powered by a second voltage different than the first voltage.

17. (Currently Amended) The electronic ~~assembly~~ system of claim 16, wherein the second voltage is less than the first voltage.

18. (Currently Amended) The electronic ~~assembly~~ system of claim 16, wherein the second voltage causes a relative delay of signals on the second interconnect as compared to signals on the first interconnect.

19. (Currently Amended) An electronic system comprising:

a memory component to store data; and

a chipset coupled to the memory component to receive the data and perform an operation on the data, wherein the chipset comprises:

a bus invert encoder circuit to receive an input data pattern for each interconnect and to provide encoding of data associated with each of the interconnects;

~~a delay circuit coupled to the bus invert encoder circuit to delay signals based on input data sampling patterns; and~~

a multi-stage interconnect including a first interconnect stage having a first interconnect and a second interconnect; and

a delay circuit coupled to the bus invert encoder circuit and the first interconnect stage to delay signals on the first interconnect as compared to signals on the second interconnect, the signals being delayed based on switching activities of signals to be applied to the first interconnect and the second interconnect.

20. (Currently Amended) The electronic ~~assembly~~ system of claim 19, wherein the multi-stage interconnect structure comprises ~~a~~ the first interconnect stage and a second interconnect stage.

21. (Currently Amended) The electronic ~~assembly~~ system of claim [[19]] 20, wherein the chipset further comprises a time-borrowing flip-flop circuit provided between the first interconnect stage and the second interconnect stage.

22. (New) The electrical system of claim 19, wherein the delay circuit delays signals on the first interconnect compared to signals on the second interconnect when there are oppositely switching signals within the signals to be applied to the first and second interconnects.

23. (New) The electrical system of claim 19, wherein the delay circuit monitors switching patterns of the signals and dynamically decides which signals to delay based on the monitored switching patterns.

24. (New) The multi-stage interconnect architecture of claim 10, wherein the delay circuit delays signals on the first one of the first plurality of parallel interconnects as compared to signals on the second one of the first plurality of parallel interconnects when there are oppositely switching signals to be applied on the first and second ones of the first plurality of parallel interconnects.

25. (New) The multi-stage interconnect architecture of claim 10, wherein the delay circuit monitors input switching patterns to be applied on the first plurality of parallel interconnects and dynamically decides which signals to delay based on the monitored input switching patterns.

26. (New) The multi-stage interconnect architecture of claim 10, wherein the delay circuit to reduce an average energy dissipation of at least the first interconnect stage.

27. (New) The apparatus of claim 6, wherein the second ones of the drivers to introduce a relative delay of signals between adjacent interconnects.

28. (New) The apparatus of claim 27, wherein the second ones of the drivers to further reduce an average energy dissipation of the interconnect structure.